

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**APPLICATION FOR LETTERS PATENT**

Title: Oxide-Nitride-Oxide Spacer with Oxide Layers Free of Nitridization

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**Field of the Invention**

The present invention relates to the field of semiconductors, and more particularly to spacer structures that include a nitride layer.

10 **Background of the Invention**

The semiconductor industry is continuously striving to reduce the size and scale of transistors in order to increase the speed and performance of microprocessors, while at the same time driving down the cost. Reductions in the scale of transistors lead to a variety of problems that require new design solutions. For instance, shrinking the size of a Metal Oxide  
15 Semiconductor Field Effect Transistor (MOSFET) reduces the distance between the source, gate, and drain, thereby increasing degradation problems resulting from various physical phenomena commonly referred to as short channel effects.

Hot carrier injection is one of the major problems encountered in scaling that is caused by very short channel lengths. It is a phenomenon that results from ballistic carrier transport,

whereby electrons traverse the channel between the source and drain while experiencing few, if any, scattering events. This ballistic transport can cause electrons to become injected into the gate oxide causing it to degrade. One design solution that compensates for hot carrier injection is a Lightly Doped Drain (LDD) MOSFET. With an LDD MOSFET, shallow implanted  
5 source/drain extensions are formed between the heavily doped source/drain regions and the channel. The reduced doping gradient provided by these shallow implanted extensions lowers the electric field in the vicinity of the drain and shifts the position of the peak electric field toward the end of channel. Carrier injection into the gate dielectric layer is thereby reduced.

LDD MOSFETS are formed using spacers. Spacers are dielectric structures that abut the  
10 gate structure of a MOSFET. Spacers function to aid in the fabrication of the shallow implanted source/drain extensions that extend between the channel and the source/drain. In addition, spacers function to electrically pacify the gate structure and insulate it from the source/drain regions. A variety of designs for spacer structures are known today in the technology. Common spacer structures known to the art include an “L” and a “D” configuration. Triangle and  
15 trapezoidal configurations are also used to form spacers. The first known method to form a spacer structure used a single layer of silicon dioxide ( $\text{SiO}_2$ ). Currently, other dielectric materials such as silicon nitride ( $\text{Si}_3\text{N}_4$ ) and silicon oxynitride ( $\text{SiON}$ ) are used to form spacers, generally in 3-layered structures.

The horizontal length,  $w$ , of the spacer at the Si interface determines the length of the  
20 LDD region, and significantly affects the device performance parameters, e.g. the value of the parasitic resistance. A key device design parameter is the ratio of the height of the gate stack  $h$  that includes the gate dielectric and electrode to the spacer width  $w$ . Referring now to Figure 1, Figure 1 shows the structure of a PRIOR ART spacer that is fabricated from a single oxide layer,

and demonstrates the initial use of a spacer for the creation of an LDD region. Also visible in Figure 1 are the gate, gate dielectric, and source/drain contact region that are formed on a substrate. With this single oxide layer spacer known to the art, the spacer width,  $w$ , is fixed by the height,  $h$ , of the gate electrode in the dry etch process since a reduction of the spacer width would entail further etching of the gate electrode. Consequently, with this prior art single oxide layer spacer, it is not possible to vary the spacer width  $w$  independently of the height  $h$ . Since the width of the LDD regions is determined by the spacer width,  $w$ , this restriction does not allow for further scaling of the LDD regions to shorter lengths that can be realized by shallow diffusion techniques. It was therefore desirable to improve upon the single oxide layer spacer known to the art and develop a spacer structure that allowed for variation of the spacer width,  $w$ , independent of the spacer height,  $h$ .

A three-layer spacer structure known to the art is shown in Figure 2. This three layer spacer structure was introduced to enable the variation of the spacer width,  $w$ , independently of the spacer height,  $h$ . This three-layer spacer has an Oxide-Nitride-Oxide (ONO) spacer structure. The three-layer spacer is formed from an initial deposition of a thin oxide layer, followed by a thin silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer, and a final layer of a relatively thick oxide. Note that commonly silicon nitride ( $\text{Si}_3\text{N}_4$ ) is simply referred to as SiN. The first oxide layer serves to isolate the silicon nitride ( $\text{Si}_3\text{N}_4$ ), or “SiN” layer from the Si surface in order to avoid degradation of device properties induced by the stress that arises at SiN/Si interfaces. The second silicon nitride, which possesses a very high etch selectivity ratio with respect to  $\text{SiO}_2$ , acts as an etch stop in the formation of the spacer. Therefore, due to the inclusion of the nitride layer, the spacer layer width,  $w$ , can be determined independent of the stack height,  $h$ , by the dry etch time parameters acting on the thick oxide layer.

Despite the advances brought about by the use of SiN in a spacer structure, which allows for a reduction of the width of the LLD region, the existing three-layer process has not addressed the deleterious effects caused by the partial nitridization of the first oxide layer. Currently, the known methods of fabricating spacer structures with nitride layers involve the use of nitride deposition processes, e.g. Low Pressure Chemical Vapor Deposition (LPCVD) or Plasma Enhanced Chemical Vapor Deposition (PECVD), that include ammonium precursors. These ammonium precursors interact with the underlying oxide layer and nitridize the oxide layer, during the so called “incubation time”, i.e. the time during which no Silicon nitride is being deposited. This nitridization of the underlying oxide layer into various forms of oxynitride during the incubation period of the deposition process causes a high stress at the silicon-oxynitride interface. The stressed interface results in the deactivation of acceptors or donors in the source/drain extension regions via a clustering mechanism, thereby causing higher series resistance with the channel in the “on” state. This higher series resistance in the extension regions gives rise to a degradation of the drive current.

It is therefore highly desirable to develop a narrow spacer structure capable of meeting current scaling demands utilizing a silicon nitride layer while avoiding the ill effects caused by nitridization of the underlying oxide layer.

### **Brief Description of the Drawings**

Figure 1 illustrates a cross-section of a PRIOR ART spacer having a single oxide layer.

Figure 2 illustrates a cross-section of a PRIOR ART spacer having an Oxide-Nitride-Oxide structure.

Figure 3 illustrates a cross-section of a MOSFET including a spacer structure formed in accordance with a present embodiment of the invention.

Figure 4 illustrates a cross-section of a spacer stack fabricated in accordance with a preferred embodiment of the present invention.

5 Figure 5 illustrates a flow chart depicting a process for fabricating the spacer stack illustrated in Figure 4.

Figure 6 illustrates a cross-section of a spacer stack fabricated in accordance with an alternative embodiment of the present invention.

10 Figure 7 illustrates a flow chart depicting a process for fabricating the spacer stack illustrated in Figure 6.

Figure 8 illustrates a cross-section of a spacer stack fabricated in accordance with an alternative embodiment of the present invention.

Figure 9 illustrates a flow chart depicting a process for fabricating the spacer stack illustrated in Figure 8.

15 Figure 10 illustrates a cross-section of a spacer stack fabricated in accordance with an alternative embodiment of the present invention.

Figure 11 illustrates a flow chart depicting a process for fabricating the spacer stack illustrated in Figure 10.

20 Figures 12-16 illustrate a series of diagrams depicting a preferred process for fabricating a spacer in accordance with a present preferred embodiment of the invention.

Figure 12 illustrates a diagram of a semiconductor wafer having a gate structure in accordance with a preferred embodiment of the present invention.

Figure 13 illustrates a diagram of a semiconductor wafer having a first spacer oxide layer deposited in accordance with a present preferred embodiment of the invention.

- 5    Figure 14 illustrates a diagram of a semiconductor wafer having a silicon nitride layer deposited over a first spacer oxide layer in accordance with a present embodiment of the invention.

Figure 15 illustrates a diagram of a semiconductor wafer having a second spacer oxide layer deposited over a silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer in accordance with a present preferred embodiment of the invention.

- 10   Figure 16 illustrates a diagram of a cross-section of a semiconductor wafer having a spacer formed in accordance with a present preferred embodiment of the invention.

### **Detailed Description of Preferred Embodiments**

- Referring to the Figures by characters of reference, Figure 3 illustrates a view of a Metal
- 15    Oxide Semiconductor Field Effect Transistor (MOSFET) having an Oxide-Nitride-Oxide spacer 2 fabricated in accordance with a preferred embodiment of the present invention. Spacer 2 is a multilayered dielectric stack structure fabricated on wafer 4. The present invention provides a novel structure and method for fabricating the nitride layer formed within Oxide-Nitride-Oxide spacer 2, which is illustrated in Figures 4-11. Spacer 2 abuts the lateral side of a gate structure 6.

Gate electrode structure 6 is fabricated over a gate dielectric layer 8. Typically, dielectric layer 8 is an oxide. Together, gate structure 6, dielectric layer 8, and wafer 4 form a Metal Oxide Semiconductor (MOS) capacitor. Operation of this MOS capacitor regulates a channel 10 that extends underneath dielectric layer 8 where current flows between the source and drain LDD regions 12 and contact regions 14 of the MOSFET.

The MOSFET illustrated in Figure 3 is a Lightly Doped Drain (LDD) MOSFET. LDD MOSFETS are fabricated having a shallow source/drain implant region 12 that extends between channel 10 and the more heavily doped source/drain contact regions 14. In an LDD MOSFET, shallow source/drain extensions 12 aid in minimizing hot carrier effects. Scaling reductions in MOSFET sizes has brought source/drain regions 12 and gate 6 contacts sufficiently close together such that ballistic transport can occur through channel 10. The reduced doping gradient provided by lightly doped source/drain extensions 12 in going between source/drain contacts 14 across channel 10 lowers the electric field in the vicinity of the drain and shifts the position of the peak electric field toward the end of channel 10. Carrier injection into dielectric layer 8 is thereby reduced.

Spacer 2 extends over these source/drain regions 12. In LDD MOSFETS, spacers 2 serve a variety of functions. Spacer 2 masks the lightly doped source drain regions 12 from the fabrication process that is used to create heavily doped source/drain contact regions 14. Heavily doped source/drain contact regions 14 are formed using a heavy implant process that is blocked from affecting lightly doped regions 12 by spacers 2. Consequently, the width,  $w$ , of spacer 2 determines the width of the lightly doped source/drain regions 12. The width,  $w$ , of lightly doped source/drain regions 12 affects the operating parameters of the MOSFET, including the parasitic resistance. Therefore, through varying the width,  $w$ , of spacers 2, it is possible to vary

the width of the lightly doped source-drain regions and in doing so, control the value of the parasitic resistance in the MOSFET.

Spacer 2 also functions to provide electrical isolation for gate structure 6 from the source and drain contacts of the MOSFET, thereby increasing device performance. In addition, spacer 2 electrically pacifies the sidewalls of gate stack 6. In the present invention, spacer 2 is formed in an “L” configuration. Alternate configurations for spacer 2 include a “D” configuration, trapezoidal, and triangular configuration.

The general structure of spacer 2 is that of an Oxide-Nitride-Oxide (ONO) spacer. The ONO structure of spacer 2 is formed with an initial deposition of a thin conformal oxide layer 16, referred to as first oxide layer 16, over wafer 4 and gate electrode 6. First oxide layer 16 functions to isolate silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18 from the Si surface of wafer 4. SiN/Si interfaces have stress that degrades device properties. First oxide layer 16 is provided to avoid the introduction of this stress by separating silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18 from the Si surface of wafer 4.

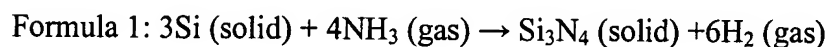
Silicon nitride ( $\text{Si}_3\text{N}_4$ ) 18 layer is formed over first oxide layer 16 to function as an etch stop. Silicon nitride ( $\text{Si}_3\text{N}_4$ ) has a very high selectivity ratio with respect to  $\text{SiO}_2$ . Therefore, with silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18, it is possible to vary the width, w, of spacer 2 independently of the height, h, of spacer 2. Consequently, it is possible to vary the width, w, of source/drain extensions 12 in order to accommodate scaling demands for shorter LDD region widths 12 that are possible with shallow diffusion techniques. A second oxide layer 20 is deposited over nitride layer 18 to complete formation of ONO spacer 2.



Spacer 2 of the present invention includes a nitride layer 18 formed with a novel spacer deposition sequence that protects underlying first oxide layer 16 from nitridization. Inhibiting the nitridization of underlying first oxide layer 16 is facilitated through providing a process for nitride deposition that does not expose first oxide layer 16 to ammonium (NH<sub>3</sub>) precursors.

5 Consequently, with the present invention, it is possible to fabricate ONO spacer structures that do not suffer from stressed interfaces, clusterization, and degradation of the drive current that are caused by nitridization of first oxide layer 16 from ammonium precursors.

Typically, nitride layer 18 is formed through a conventional silicon nitride (Si<sub>3</sub>N<sub>4</sub>) plasma process that can include ammonium precursors. The chemical formula for fabricating nitride  
10 layer 18 with ammonium precursors is given by Formula 1 below:



Conventional thermal silicon nitride (Si<sub>3</sub>N<sub>4</sub>) plasma processes that include ammonium precursors can nitridize oxide layers, such as layer 16, if the oxide layers are exposed to the ammonium precursors. Nitridization of oxide layers converts the layer to oxynitride as given by Formula 2  
15 below:



This nitridized oxide film 16 causes stress at the silicon-oxynitride interface, as well as at the “corner” of the gate oxide adjacent to the spacer oxide 16. The stress at the gate corner region is a feature size stress. The stress located in the gate region can cause degradation of  
20 device performance parameters. The stress at the silicon-oxynitride interface is an atomic scale of stress. The width, w, of spacer 2 determines the depth of stress penetration into substrate 4.

The stressed interface at the LLD regions 12 results in the deactivation of acceptors or donors in source/drain regions 12 via a clustering mechanism. This deactivation causes a higher series resistance in the source/drain extensions 12 and degrades the drive current. One method of accounting for the deactivation of dopants is through increasing the dopant dose in advance.

5 However, this compensation through a higher dopant dose results in an increase in the depth of the LDD extensions 12. Ultimately, this compensation leads to deterioration of the MOSFET device performance due to Short Channel Effects (SCE). In addition, the stress at the LLD region can result in further degradation in device properties via a junction leakage mechanism.

Referring again to Figure 3, the circled portion of spacer 2, designated as 1-1, identifies a  
10 cross-section of the spacer stack that forms spacer 2. The spacer stack is a stack of layered materials, which form spacer 2. The present invention provides a novel structure and method for fabricating silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18 within the spacer stack to inhibit the nitridization of oxide layer 16 and avoid the problems associated with nitridization. Preferred and alternate embodiments of the present invention for the novel spacer stacks that form spacer 2 are  
15 illustrated in Figures 4, 6, 8, and 10. Processes for forming the preferred and alternate embodiments of the spacer stacks of the present invention are illustrated in Figures 5, 7, 9, and 11 respectively.

Figure 4 illustrates a cross-section of a spacer stack that forms spacer 2 fabricated in accordance with a preferred embodiment of the present invention. The spacer stack of Figure 4  
20 has an ONO structure. The base layer of spacer stack is an oxide layer 16 that is deposited over wafer 4. A silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18 is deposited over oxide layer 16. SiN/Si interfaces have a high level of stress that leads to degradation of device performance. Through providing oxide layer 16 between silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18 and Si wafer 4, the creation of a SiN/Si

interface is prevented and introduction of this stress is avoided. A second oxide layer 20 is then deposited over silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer to complete the ONO structure.

In accordance with a preferred embodiment of the present invention, a novel structure and process for fabrication of silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18 is provided to avoid nitridization of oxide layer 16, thereby enhancing device performance. Silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18 is fabricated through a process that does not expose oxide layer 16 to ammonium precursors, thereby preventing its nitridization. A barrier layer of nitride 22 is deposited over oxide layer 16 through an Atomic Layer Deposition (ALD) process. This ALD process does not include the use of ammonium precursors. Since ammonium precursors are not used to deposit barrier layer of nitride 22, oxide layer 16 is not nitridized during this process.

An etch stop layer of nitride 24 is deposited over barrier layer of nitride 22 through a conventional deposition process that includes the use of ammonium precursors. Etch stop layer of nitride 24 is formed in order to provide a barrier to the etching process used to shape spacer 2. Due to the presence of barrier layer of nitride 22, oxide layer 16 is not exposed to the ammonium precursors used to form etch stop layer of nitride 24 since ammonium precursors cannot easily diffuse through nitride. An exemplary thickness for barrier nitride layer 22 is 1.5 to 3.0 nm. An exemplary thickness for etch stop layer 24 is 30 to 90 nm.

Barrier silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 22 functions as barrier protecting oxide layer 16 from the ammonium precursors present in the plasma process that forms layer 24 as given by Formula 1. Barrier silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 22 is formed through a nitride deposition process that does not include the presence of ammonium precursors. Consequently, the deposition of barrier silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 22 does not nitridize first oxide layer 16. Once barrier silicon nitride

(Si<sub>3</sub>N<sub>4</sub>) layer 2 is deposited, subsequent deposition of layer 24 with ammonium precursors can occur. Barrier silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 22 blocks the ammonium precursors used in the process to deposit layer 24 from interacting with and nitridizing oxide layer 16. Through inhibiting formation of a silicon-oxynitride interface, barrier silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 22  
5 deters formation of interface stresses that cause deactivation of acceptors or donors in source/drain regions 12 via the clustering mechanism. Consequently, this structure having barrier silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 22 facilitates the inclusion of nitride layer 18 with spacer 2 without causing higher series resistance in source/drain extensions 12 and without degradation of the drive current.

10 When compared to conventional nitride deposition processes that include ammonium precursors, ALD processes take longer periods of time to complete and are more expensive. It is therefore desirable to continue to utilize conventional nitride deposition processes to form the relatively thick 30 to 90 nm etch stop layer of nitride 24 after formation of the initial barrier nitride layer 22.

15 Through formation of barrier nitride layer 22 and etch stop nitride layer 24, it is possible to fabricate a silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 18 that utilizes cost effective nitride deposition techniques without nitridizing oxide layer 16, thereby enhancing the device performance.

Figure 5 illustrates a flow chart 100 depicting a process for fabricating spacer stack illustrated in Figure 4. In step 102, first spacer oxide layer 16 is deposited through a  
20 conventional CVD or PECVD process. In the process illustrated by Figure 5, nitride layer 18 is formed through a two-step process. In step 104, barrier silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 22 is deposited over first oxide layer 16. A preferred method of fabricating barrier silicon nitride

(Si<sub>3</sub>N<sub>4</sub>) layer 22 is through an Atomic Layer Deposition (ALD) process. An exemplary thickness for barrier silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 22 is 1.5nm to 3nm.

After the fabrication of barrier silicon nitride layer 22 in step 104, the process proceeds to step 106 where etch stop silicon nitride layer 24 is deposited. It is possible to form etch stop silicon nitride layer 24 through a variety of processes, including conventional CVD type deposition processes using ammonium precursors. In step 108, second spacer oxide 20 is deposited over etch stop silicon nitride layer 24 through either a CVD or PECVD process. Finally in step 110, an etching process is used to remove unwanted portions of layers 16, 18, and 20 deposited in the previous steps in order to fabricate spacer 2 with a desired width, w, and a height h.

Figure 6 illustrates a cross-section of a spacer stack fabricated for spacer 2 in accordance with an alternative embodiment of the present invention. The spacer stack of Figure 6 includes nitride layer 18 formed between two oxide layers 16 and 20, thereby forming an ONO structure. Nitride layer 18 is formed from a barrier nitride layer 26 and an etch stop layer of nitride 28. In this alternative embodiment of the invention, barrier nitride layer 26 is formed through a Plasma Enhanced Chemical Vapor Deposition (PECVD) process utilizing N<sub>2</sub> and SiCl<sub>4</sub> or SiF<sub>4</sub> or other H-free Si-carrying precursors. Another way of forming barrier nitride layer 26 in this embodiment is through Jet Vapor Deposition (JVD) or N-Si-radical contained in organic precursors, e.g. tertiary-butyl amino silane (BTBAS). Since ammonium precursors are not used to form barrier nitride layer 26, oxide layer 16 is not nitridized. Subsequent deposition of etch stop layer of nitride 28 through conventional nitride deposition processes that include ammonium precursors are then possible due to the fact that barrier nitride layer 26 blocks the ammonium precursors from reaching oxide layer 16. Therefore, as with the preferred embodiment, this

alternative embodiment facilitates the use of conventional deposition processes to form the relatively thick nitride etch stop layer 28 without exposing oxide layer 16 to nitridization through the formation of barrier nitride layer 26.

Figure 7 illustrates a flow chart 200 depicting a process for fabricating the spacer stack illustrated in Figure 6. In step 202, first spacer oxide layer 16 is deposited through a conventional CVD or PECVD process. In the process illustrated by Figure 7, nitride layer 18 is formed through a two-step process. In step 104, barrier silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 26 is deposited over first oxide layer 16. One method of fabricating barrier silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 26 as illustrated in Figure 6 is through a Plasma Enhanced Chemical Vapor Deposition (PECVD) process utilizing  $\text{N}_2$  and  $\text{SiCl}_4$  or  $\text{SiF}_4$  components without ammonium precursors. Another way of forming barrier nitride layer 26 in this embodiment is through Jet Vapor Deposition (JVD) or N-Si-radical containing in an organic precursors, e.g. tertiary-butyl amino silane (BTBAS). An exemplary thickness for barrier silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 26 is 1.5nm to 10nm or even up to the total  $\text{Si}_3\text{N}_4$  thickness if a process is optimized to provide a good  $\text{Si}_3\text{N}_4$  quality and a practical rate of deposition.

After the fabrication of barrier silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 26 in step 204, the process proceeds to step 206 where etch stop silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 24 is deposited. It is possible to form etch stop silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 24 through a variety of processes, including conventional CVD type deposition processes using ammonium precursors. In step 208, second oxide layer 20 is deposited over etch stop silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 28 through either a CVD or PECVD process. Finally in step 210, an etching process is used to remove unwanted portions of layers 16, 18, and 20 deposited in the previous steps in order to fabricate spacer 2 with a width, w, and a height h. Since ammonium precursors are not used to form barrier nitride layer

26, oxide layer 16 is not nitridized. Subsequent deposition of etch stop layer of nitride 28 through conventional nitride deposition processes that include ammonium precursors are then possible due to the fact that barrier nitride layer 26 blocks the ammonium precursors from reaching oxide layer 16. If the total  $\text{Si}_3\text{N}_4$  thickness can be done by the first step, the second step  
5 can be omitted to simplify the process.

Figure 8 illustrates a cross-section of a spacer stack fabricated in accordance with an alternative embodiment of the present invention. In this alternative embodiment of the invention, nitride layer 18 also includes a barrier nitride layer 30 and a nitride etch stop layer 32. Barrier nitride layer 30 is formed through an initial deposition of a thin silicon layer 30 of 1 to 2  
10 nm of amorphous, or poly-silicon using ALD, JVD, or other processes that allow for such deposition of very thin layers. This layer 30 of amorphous, or poly-silicon is then nitridized through a plasma process. The nitridization of amorphous Si is a self-limiting process because the nitridization precursors are limited by diffusion through the ever-increasing thickness of the converted nitride layer. Therefore, no contamination, i.e. formation of oxynitride, in the  
15 underlying oxide can occur. This alternative embodiment for the formation of a spacer structure with barrier nitride layer 30 formed with nitridized amorphous, or poly-silicon allows for the formation of an ONO structure without the nitridization of oxide layer 16. Conventional nitride deposition processes deposit second nitride layer 32. These plasma processes can include ammonium precursors, thereby making formation of barrier nitride layer 30 and nitride etch stop  
20 layer 32 relatively fast and economical.

Figure 9 illustrates a flow chart 300 depicting a process for fabricating the spacer stack illustrated in Figure 8. In step 302, first spacer oxide layer 16 is deposited through a conventional CVD or PECVD process. In the process illustrated by Figure 9, nitride layer 18 is

formed through a two-step process. The method of fabricating barrier silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18 as illustrated in Figure 8 is through an initial deposition of a layer 30 of 1 to 2 nm of amorphous, or poly-silicon in step 304. In step 306, this layer 30 of amorphous, or poly-silicon is then nitridized through a plasma process. A second process 308 is used to deposit the final etch stop nitride layer 32. With this second process in step 310, second spacer oxide 20 is deposited over etch stop silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 32 through either a CVD or PECVD process. Finally in step 312, an etching process is used to remove unwanted portions of the layers 16, 18, and 20 deposited in the previous steps in order to fabricate spacer 2 with a width, w, and a height h. Since nitridization is a self-limiting process, the ammonium precursors used in the plasma process to convert amorphous, or poly-silicon Si layer 30 into the nitride barrier layer 30, are prevented from nitridizing the oxide layer 16, since they are unable to penetrate the nitride layer as it is formed in the diffusion limited process. Therefore, an ONO spacer 2 is fabricated that does not suffer from the ill effects caused by nitridization of oxide layer 16.

Figure 10 illustrates a cross-section of a spacer stack fabricated in accordance with an alternative embodiment of the present invention. In this alternative embodiment, the spacer stack is formed having a silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18/38 formed through a single ALD process. The entire thickness of silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18/38 is formed through deposition of nitride through the ALD process. Since deposition of nitride with ALD does not utilize ammonium precursors, oxide layer 16 is not nitridized.

Figure 11 illustrates a flow chart 400 depicting a process for fabricating the spacer stack illustrated in Figure 10. In step 402, first oxide layer 16 is deposited through a conventional CVD or PECVD process. In step 404, silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18/38 is deposited over first oxide layer 16. The method of fabricating first silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18/38 as illustrated in



Figure 10 is through an Atomic Layer Deposition of silicon nitride ( $\text{Si}_3\text{N}_4$ ) that does not include the use of ammonium precursors. An exemplary thickness for first silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18/38 is 30 nm to 90 nm. Note that in this process, the entire nitride layer 18/38 is formed through a single process.

5        After the fabrication of silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18/38 in step 404, the process proceeds to step 306 where second oxide layer 20 is deposited over silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 18/38 through either a CVD or PECVD process. Finally in step 406, an etching process is used to remove unwanted portions of the layers 16, 18, and 20 deposited in the previous steps in order to fabricate spacer 2 with a width, w, and a height h. Since ammonium precursors are not used to  
10    form nitride layer 18/38, oxide layer 16 is not nitridized.

Figures 12-16 illustrate a series of diagrams depicting a preferred process for fabricating spacer 2 in accordance with a present preferred embodiment of the invention.

Figure 12 illustrates an initial fabrication stage where a gate structure 6 is formed over a gate dielectric layer 8 on top of a wafer 4. Dielectric layer 8 is typically formed from silicon  
15    dioxide. Exemplary materials for the electrode in gate structure 6 are polysilicon and metal. At this stage, as illustrated in Figure 3, lightly doped source/drain extensions 12 are formed using a light implant process 42.

Figure 13 illustrates fabrication of first oxide layer 16 on to wafer 4. It is possible to form first oxide layer 16 from a variety of deposition processes including Chemical Vapor  
20    Deposition (CVD) and Plasma Enhanced Chemical Vapor Deposition (PECVD). An exemplary material for first spacer oxide layer 16 is TEOS (Tetraethoxysilane). TEOS is a gaseous compound commonly used in CVD  $\text{SiO}_2$  processes that conforms well to the underlying surface.

Figure 14 illustrates a diagram of a semiconductor wafer 4 having silicon nitride (SiN) layer 18 deposited over first spacer oxide layer 16 in accordance with a present embodiment of the invention as described in Figures 4-11. Silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 18 provides a protective layer for first oxide layer 16 to guard against nitridization by fabrication processes that involve the use of ammonium precursors.

Figure 15 illustrates a diagram of semiconductor wafer 4 having second oxide layer 20 deposited over second silicon nitride (SiN) layer 18 accordance with a present preferred embodiment of the invention. Second oxide layer 20 is deposited through a conventional CVD or PECVD process.

Figure 16 illustrates a diagram of a cross-section of semiconductor wafer 4 having spacer 2 formed in accordance with a present preferred embodiment of the invention. At this stage of fabrication, etching processes are used in order to form spacers 2 with a desired width, w, and height, h. The width, w, of spacers 2 determines the width, w, of lightly doped regions 12. A subsequent heavy implant process 44 is then used in order to create source/drain contact regions 14.

Having fully described the invention with referred to the preferred embodiments illustrated in the attached drawing Figures, it will be really appreciated by those skilled in the art that many changes and modifications may be made to the invention without departing from the essence of the invention and without being included within the spirit and scope of the invention as is defined by the appended claims.